What is claimed is:

1. A capacitor, comprising:

a first plate of conductive material formed in a predetermined shape;

a layer of dielectric material formed on at least a portion of the first plate and substantially conforming to the predetermined shape of the first plate; and

a second plate of conductive material formed over the layer of dielectric material.

2. The capacitor of claim 1, wherein the conductive material of the first plate comprises a metal or a semiconductor.

3. The capacitor of claim 1, wherein the layer of dielectric material comprises any dielectric.

4. The capacitor of claim 1, wherein the predetermined shape of the first conductive layer has a depth larger than a width.

5. The capacitor of claim 1, wherein the open interior portion of the first layer has a substantially elliptical cross-section.

6. The capacitor of claim 1, wherein the open interior portion of the first plate has a substantially circular cross-section.

7. The capacitor of claim 1, wherein the first plate of conductive material is thicker than the layer of dielectric material.

8. The capacitor of claim 1, wherein the first plate of conductive material has a thickness of about 300 angstroms.

9. The capacitor of claim 1, wherein the layer of dielectric material has a predetermined thickness.

10. A capacitor, comprising:

a first plate of conductive material formed in a predetermined shape with an open interior portion, wherein at least one of an interior surface and at least a portion of an exterior surface of the first plate are converted into hemispherical grains;

a layer of dielectric material formed on at least a portion of the first plate and substantially conforming to the predetermined shape of the first plate; and

a second plate of conductive material formed over the layer of dielectric material.

11. A capacitor, comprising:

a substantially cone-shaped first plate of conductive material;

a layer of dielectric material formed on at least a portion of the first plate and substantially conforming to the shape of the first plate; and

a second plate of conductive material formed over the layer of dielectric material.

12. A capacitor, comprising:

a substantially cone-shaped first plate of conductive material with a hollow interior portion, wherein at least one of an interior surface and at least a portion of an exterior surface of the first plate are converted into hemispherical grains;

a layer of dielectric material formed on at least a portion of the substantially cone-shaped first plate and substantially conforming to the shape of the first plate and the hemispherical grains; and

a second plate of conductive material formed over the layer of dielectric material.

13. A capacitor, comprising:

a layer of forming material;

a first plate of conductive material formed in a predetermined shape including an open interior portion and a closed end extending partially into the layer of forming material;

a layer of dielectric material formed on an interior surface and an exposed exterior surface of the first plate extending outside of the layer of forming material, wherein the layer of dielectric material substantially conforms to the shape of the first plate; and

a second plate of conductive material formed over the layer of dielectric material.

14. A capacitor, comprising:

a layer of forming material;

a substantially cone-shaped first plate of conductive material including a vertex portion extending partially into the layer of forming material;

a layer of dielectric material formed on an interior surface and an exposed exterior surface of the first plate extending outside of the layer of forming material, wherein the layer of dielectric material substantially conforms to the shape of the first plate; and

a second plate of conductive material formed over the layer of dielectric material.

15. The capacitor of claim 14, wherein the layer of forming material comprises a layer of dielectric material.

16. The capacitor of claim 14, wherein the layer of forming material comprises a layer of oxide.

17. A capacitor, comprising:

a layer of forming material;

a substantially cone-shaped first plate of conductive material including a vertex portion extending partially into the layer of forming material, wherein at least one of an interior surface and an exterior surface of the first plate exposed outside of the layer of forming material is converted into hemispherical grains;

a layer of dielectric material formed on the interior surface and the exposed exterior surface of the first plate, wherein the layer of dielectric material substantially conforms to the shape of the first plate and the hemispherical grains; and

a second plate of conductive material formed over the layer of dielectric material.

18. A capacitor, comprising:

a layer of forming material;

a nucleation layer formed on the layer of forming material;

a substantially cone-shaped first plate of conductive material including a vertex portion extending through the nucleation layer and partially into the layer of forming material;

a layer of dielectric material formed on the nucleation layer and on an interior surface and an exposed exterior surface of the first plate extending out of the layer of forming material and the nucleation layer, wherein the layer of dielectric material substantially conforms to the shape of the first plate; and

a second plate of conductive material formed over the layer of dielectric material.

19. The capacitor of claim 18, wherein the layer of forming material comprises a layer of doped oxide.

20. The capacitor of claim 18, wherein the nucleation layer comprises a layer of undoped oxide.

21. A capacitor, comprising:

a layer of forming material;

a nucleation layer formed on the layer of forming material;

a substantially cone-shaped first plate of conductive material including a vertex portion extending through the nucleation layer and partially into the layer of forming material, wherein at least one of an interior surface and an exposed exterior surface of the first plate extending from the layer of forming material and the nucleation layer is converted into hemispherical grains;

a layer of dielectric material formed on the nucleation layer and on the interior surface and the exposed exterior surface of the first plate, wherein the layer of dielectric material substantially conforms to the shape of the first plate and the hemispherical grains; and

a second plate of conductive material formed over the layer of dielectric material.

22. A capacitor, comprising:

a layer of forming material;

an electrode formed in the layer of forming material;

a nucleation layer formed on the layer of forming material;

a substantially cone-shaped first plate of conductive material including a vertex portion extending through the nucleation layer and partially into the layer of forming material and in contact with the electrode;

a layer of dielectric material formed on the nucleation layer and on an interior surface and on an exposed exterior surface of the first plate extending out of the layer of forming material and the nucleation layer, wherein the layer of dielectric material substantially conforms to the shape of the first plate; and

a second plate of conductive material formed over the layer of dielectric material.

23. A capacitor, comprising:

a layer of forming material;

an electrode formed in the layer of forming material;

a nucleation layer formed on the layer of forming material;

a substantially cone-shaped first plate of conductive material including a vertex portion extending through the nucleation layer and partially into the layer of forming material and in contact with the electrode, wherein at least one of an interior surface and an exposed exterior surface of the first plate extending from the layer of forming material and the nucleation layer is converted into hemispherical grains;

a layer of dielectric material formed on the nucleation layer and on the interior surface and the exposed exterior surface of the first plate, wherein the layer of dielectric material substantially conforms to the shape of the first plate and the hemispherical grains; and

a second plate of conductive material formed over the layer of dielectric material.

24. An array of capacitors, comprising:

a plurality of first plates of conductive material, each formed in a predetermined shape with an open interior portion;

a layer of dielectric material formed on the plurality of first plates and substantially conforming to the shape of each of the first plates; and

a second plate of conductive material formed over the layer of dielectric material.

25. An array of capacitors, comprising:

a plurality of substantially cone-shaped first plates of conductive material, wherein at least one of an interior surface and at least a portion of an exterior surface of each of the first plates are converted into hemispherical grains;

a layer of dielectric material formed on at least a portion of each of the plurality of first plates and substantially conforming to the shape of each of the first plates and the hemispherical grains; and

a second plate of conductive material formed over the layer of dielectric material.

26. An array of capacitors, comprising:

a layer of forming material;

a plurality of substantially cone-shaped first plates of conductive material, each including a vertex portion extending partially into the layer of forming material;

a layer of dielectric material formed on an interior surface and an exposed exterior portion of each of the plurality of first plates extending outside of the layer of forming material, wherein the layer of dielectric material substantially conforms to the shape of each first plate; and

a second plate of conductive material formed over the layer of dielectric material.

27. An array of capacitors, comprising:

a layer of forming material;

a plurality of substantially cone-shaped first plates of conductive material, each including a vertex portion extending partially into the layer of forming material, wherein at least one of an interior surface and an exterior surface of each first plate exposed outside of the layer of forming material is converted into hemispherical grains;

a layer of dielectric material formed on the interior surface and the exposed exterior surface of each first plate, wherein the layer of dielectric material substantially conforms to the shape of each first plate and the hemispherical grains; and

a second plate of conductive material formed over the layer of dielectric material.

28. An array of capacitors, comprising:

a layer of forming material;

a nucleation layer formed on the layer of forming material;

a plurality of substantially cone-shaped first plates of conductive material, each including a vertex portion extending through the nucleation layer and partially into the layer of forming material;

a layer of dielectric material formed on the nucleation layer and on an interior surface and an exposed exterior surface of each first plate extending out of the layer of forming material and the nucleation layer, wherein the layer of dielectric material substantially conforms to the shape of each first plate; and

a second plate of conductive material formed over the layer of dielectric material.

29. A memory system, comprising:

at least one memory element including a capacitor, thecapacitor including:

a first plate of conductive material formed in a predetermined shape,

a layer of dielectric material formed on at least a portion of the first plate and substantially conforming to the shape of the first plate, and

a second plate of conductive material formed over the layer of dielectric material.

30. The memory system of claim 29, wherein the first plate comprises at least one of a metal and a semiconductor material.

31. The memory system of claim 29, wherein the layer of dielectric material comprises one of a nitride layer and an oxide layer.

32. The memory system of claim 29, wherein the substantially cone-shaped first plate has a substantially elliptical cross-section.

33. A memory system, comprising:

an array of memory elements, each memory element including a capacitor and each capacitor including:

a substantially cone-shaped first plate of conductive material,

a layer of dielectric material formed on at least a portion of the first plate and substantially conforming to the shape of the first plate, and

a second plate of conductive material formed over the layer of dielectric material.

34. A memory system, comprising:

an array of memory elements, each memory element including a capacitor and each capacitor including:

a substantially cone-shaped first plate of conductive material, wherein at least one of an interior surface and at least a portion of an exterior surface of the first plate are converted into hemispherical grains,

a layer of dielectric material formed on at least a portion of the substantially cone-shaped first plate and substantially conforming to the shape of the first plate and the hemispherical grains, and

a second plate of conductive material formed over the layer of dielectric material.

35. A memory system, comprising:

an array of memory elements, each memory element including a capacitor and each capacitor including:

a layer of forming material,

a substantially cone-shaped first plate of conductive material including a vertex portion extending partially into the layer of forming material,

a layer of dielectric material formed on an interior surface and an exposed exterior portion of the first plate extending outside of the layer of forming material, wherein the layer of dielectric material substantially conforms to the shape of the first plate, and

a second plate of conductive material formed over the layer of dielectric material.

36. A memory system, comprising:

an array of memory elements, each memory element including a capacitor and each capacitor including:

a layer of forming material,

a nucleation layer formed on the layer of forming material,

a substantially cone-shaped first plate of conductive material including a vertex portion extending through the nucleation layer and partially into the layer of forming material,

a layer of dielectric material formed on the nucleation layer and on an interior surface and an exposed exterior surface of the first plate extending out of the layer of forming material and the nucleation layer, wherein the layer of dielectric material substantially conforms to the shape of the first plate, and

a second plate of conductive material formed over the layer of dielectric material.

37. A memory system, comprising:

an array of memory elements arranged in rows and columns;

a plurality of address lines each coupled to one of a row or a column of memory elements; and

a plurality of data lines each coupled to one of a row or a column of memory elements, each memory element including:

a transistor including a gate terminal coupled to an address line and a source/drain terminal coupled to a data line; and

a capacitor coupled to another source/drain terminal, wherein the capacitor includes:

a layer of forming material,

a nucleation layer formed on the layer of forming material,

a substantially cone-shaped first plate of conductive material including a vertex portion extending through the nucleation layer and partially into the layer of forming material, wherein at least one of an interior surface and an exposed exterior surface of the first plate extending from the layer of forming material and the nucleation layer is converted into hemispherical grains,

a layer of dielectric material formed on the nucleation layer and on the interior surface and the exposed exterior surface of the first plate, wherein the layer of dielectric material substantially conforms to the shape of the first plate and the hemispherical grains, and

a second plate of conductive material formed over the layer of dielectric material.

38. A semiconductor die, comprising:

a substrate; and

an integrated circuit formed supported by the substrate, wherein the integrated circuit comprises at least one capacitor, the at least one capacitor including:

a first plate of conductive material formed in a predetermined shape,

a layer of dielectric material formed on at least a portion of the first plate and substantially conforming to the shape of the first plate, and

a second plate of conductive material formed over the layer of dielectric material.

39. A semiconductor die, comprising:

a substrate; and

an integrated circuit supported by the substrate, wherein the integrated circuit comprises at least one capacitor, the at least one capacitor including:

a substantially cone-shaped first plate of conductive material, wherein at least one of an interior surface and at least a portion of an exterior surface of the first plate are converted into hemispherical grains,

a layer of dielectric material formed on at least a portion of the substantially cone-shaped first plate and substantially conforming to the shape of the first plate and the hemispherical grains, and

a second plate of conductive material formed over the layer of dielectric material.

40. A semiconductor die, comprising:

a substrate; and

an integrated circuit formed on the substrate, wherein the integrated circuit comprises at least one capacitor, the at least one capacitor including:

a layer of forming material,

a substantially cone-shaped first plate of conductive material including a vertex portion extending partially into the layer of forming material,

a layer of dielectric material formed on an interior surface and an exposed exterior portion of the first plate extending outside of the layer of forming material, wherein the layer of dielectric material substantially conforms to the shape of the first plate, and

a second plate of conductive material formed over the layer of dielectric material.

41. A semiconductor die, comprising:

a substrate; and

an integrated circuit formed on the substrate, wherein the integrated circuit comprises an array of capacitors, including:

a layer of forming material,

a plurality of substantially cone-shaped first plates of conductive material, each including a vertex portion extending partially into the layer of forming material, wherein at least one of an interior surface and an exterior surface of each first plate exposed outside of the layer of forming material is converted into hemispherical grains,

a layer of dielectric material formed on the interior surface and the exposed exterior surface of each first plate, wherein the layer of dielectric material substantially conforms to the shape of each first plate and the hemispherical grains, and

a second plate of conductive material formed over the layer of dielectric material.

42. A semiconductor die, comprising:

a substrate; and

an integrated circuit formed on the substrate, wherein the integrated circuit comprises an array of capacitors, including:

a layer of forming material,

a nucleation layer formed on the layer of forming material,

a plurality of substantially cone-shaped first plates of conductive material, each including a vertex portion extending through the nucleation layer and partially into the layer of forming material,

a layer of dielectric material formed on the nucleation layer and on an interior surface and an exposed exterior surface of each first plate extending out of the layer of forming material and the nucleation layer, wherein the layer of dielectric material substantially conforms to the shape of each first plate, and

a second plate of conductive material formed over the layer of dielectric material.

43. A semiconductor die, comprising:

a substrate; and

an integrated circuit formed on the substrate, wherein the integrated circuit comprises an array of capacitors, including:

a layer of forming material,

a plurality of electrodes formed in the layer of forming material,

a plurality of substantially cone-shaped first plates of conductive material, each including a vertex portion extending partially into the layer of forming material and each in contact with a corresponding one of the plurality of electrodes,

a layer of dielectric material formed on an interior surface and an exposed exterior portion of each of the plurality of first plates extending outside of the layer of forming material, wherein the layer of dielectric material substantially conforms to the shape of each first plate, and

a second plate of conductive material formed over the layer of dielectric material.

44. An electronic system, comprising:

a processor; and

a memory system coupled to the processor, the memory system comprising an array of memory elements and each memory element including a capacitor, each capacitor including:

a first plate of conductive material formed in a predetermined shape,

a layer of dielectric material formed on at least a portion of the first plate and substantially conforming to the shape of the first plate, and

a second plate of conductive material formed over the layer of dielectric material.

45. An electronic system, comprising:

a processor; and

a memory system coupled to the processor, the memory system comprising at least one memory element including a capacitor, each capacitor including:

a substantially cone-shaped first plate of conductive material,

a layer of dielectric material formed on at least a portion of the first plate and substantially conforming to the shape of the first plate, and

a second plate of conductive material formed over the layer of dielectric material.

46. An electronic system, comprising:

a processor; and

a memory system coupled to the processor, the memory system comprising an array of memory elements and each memory element including a capacitor, each capacitor including:

a substantially cone-shaped first plate of conductive material, wherein at least one of an interior surface and at least a portion of an exterior surface of the first plate are converted into hemispherical grains,

a layer of dielectric material formed on at least a portion of the substantially cone-shaped first plate and substantially conforming to the shape of the first plate and the hemispherical grains, and

a second plate of conductive material formed over the layer of dielectric material.

47. An electronic system, comprising:

a processor; and

a memory system coupled to the processor, the memory system comprising an array of memory elements and each memory element including a capacitor, each capacitor including:

a layer of forming material,

a substantially cone-shaped first plate of conductive material including a vertex portion extending partially into the layer of forming material,

a layer of dielectric material formed on an interior surface and an exposed exterior portion of the first plate extending outside of the layer of forming material, wherein the layer of dielectric material substantially conforms to the shape of the first plate, and

a second plate of conductive material formed over the layer of dielectric material.

48. An electronic system, comprising:

a processor; and

a memory system coupled to the processor, the memory system comprising an array of memory elements and each memory element including a capacitor, each capacitor including:

a layer of forming material,

a nucleation layer formed on the layer of forming material,

a substantially cone-shaped first plate of conductive material including a vertex portion extending through the nucleation layer and partially into the layer of forming material,

a layer of dielectric material formed on the nucleation layer and on an interior surface and an exposed exterior surface of the first plate extending out of the layer of forming material and the nucleation layer, wherein the layer of dielectric material substantially conforms to the shape of the first plate, and

a second plate of conductive material formed over the layer of dielectric material.

49. An electronic system, comprising:

a processor; and

a memory system coupled to the processor, the memory system comprising:

an array of memory elements arranged in rows and columns;

a plurality of address lines each coupled to one of a row or a column of memory elements; and

a plurality of data lines each coupled to one of a row or a column of memory elements, each memory element including:

a transistor including a gate terminal coupled to an address line and a source/drain terminal coupled to a data line; and

a capacitor coupled to another source/drain terminal, wherein the capacitor includes:

a layer of forming material,

a nucleation layer formed on the layer of forming material,

a substantially cone-shaped first plate of conductive material including a vertex portion extending through the nucleation layer and partially into the layer of forming material, wherein at least one of an interior surface and an exposed exterior surface of the first plate extending from the layer of forming material and the nucleation layer is converted into hemispherical grains,

a layer of dielectric material formed on the nucleation layer and on the interior surface and the exposed exterior surface of the first plate, wherein the layer of dielectric material substantially conforms to the shape of the first plate and the hemispherical grains, and

a second plate of conductive material formed over the layer of dielectric material.

50. An electronic system, comprising:

a processor; and

a memory system coupled to the processor, the memory system comprising an array of memory elements and each memory element including a capacitor, each capacitor including:

a layer of forming material,

an electrode formed in the layer of forming material,

a substantially cone-shaped first plate of conductive material including a vertex portion extending partially into the layer of forming material and in contact with the electrode,

a layer of dielectric material formed on the nucleation layer and on an interior surface and on an exposed exterior surface of the first plate extending out of the layer of forming material and the nucleation layer, wherein the layer of dielectric material substantially conforms to the shape of the first plate, and

a second plate of conductive material formed over the layer of dielectric material.

51. A method of making a capacitor, comprising:

forming a substantially cone-shaped first plate of conductive material;

forming a layer of dielectric material on at least a portion of the first plate and substantially conforming to the shape of the first plate; and

forming a second plate of conductive material over the layer of dielectric material.

52. A method of making a capacitor, comprising:

forming a layer of forming material;

forming at least one cavity with a predetermined shape in a surface of the layer of forming material;

forming a first plate of conductive material on the layer of forming material and in the at least one cavity, wherein the first plate of conductive material forms a

predetermined shape substantially conforming to the shape of the cavity with a hollow interior surface;

removing the layer of forming material to a predetermined level to expose at least a portion of an exterior surface of the first plate above a remaining portion of the layer of forming material;

forming a layer of dielectric material on the first plate substantially conforming to the shape of the first plate; and

forming a second plate of conductive material over the layer of dielectric material.

53. The method of claim 52, wherein removing the layer of forming material comprises:

removing a portion of the first plate from a surface of the forming material surrounding the cavity by dry etching the first layer with an etchant that is non-reactive to the forming material.

54. The method of claim 52, wherein removing the layer of forming material comprises wet etching with an etchant that is non-reactive to the first plate of conductive material.

55. The method of claim 52, wherein forming the layer of dielectric material comprises forming a layer of one of a nitride or an oxide.

56. A method of making a capacitor, comprising:

forming a first layer of forming material;

forming a nucleation layer on the first layer of forming material;

forming a second layer of forming material on the nucleation layer;

forming at least one cavity with a predetermined shape in the first layer of forming material, the nucleation layer and the second layer of forming material;

forming a first plate of conductive material on the second layer of forming material and in the at least one cavity, wherein the first layer of conductive material forms a predetermined shape substantially conforming to the shape of the cavity with a hollow interior surface;

removing the first plate of conductive material from the surface of the second layer of forming material around the cavity;

removing the second layer of forming material to expose the nucleation layer and to expose at least a portion of an exterior surface of the first plate of conductive material extending above of the nucleation layer;

forming a layer of dielectric material on the first plate that substantially conforms to the shape of the first plate; and

forming a second plate of conductive material over the layer of dielectric material.

57. The method of claim 56, wherein forming the second layer of forming material comprises forming a layer of doped oxide.

58. The method of claim 56, wherein forming the nucleation layer comprises forming a layer of undoped oxide.

59. A method of making a capacitor, comprising:

forming a first layer of forming material;

forming a nucleation layer on the first layer of forming material;

forming a second layer of forming material on the nucleation layer;

forming at least one cavity with a predetermined shape in the first layer of forming material, the nucleation layer and the second layer of forming material;

forming a first plate of conductive material on the second layer of forming material and in the at least one cavity, wherein the first layer of conductive material forms a predetermined shape substantially conforming to the shape of the cavity with a hollow interior surface;

removing the first plate of conductive material from the surface of the second layer of forming material around the cavity;

removing the second layer of forming material to expose the nucleation layer and to expose at least a portion of an exterior surface of the first plate of conductive material extending above of the nucleation layer;

converting at least one of an interior surface and an exterior surface of the first plate exposed above the nucleation layer to hemispherical grains;

forming a layer of dielectric material on the first plate substantially conforming to the shape of the first plate and the hemispherical grains; and

forming a second plate of conductive material over the layer of dielectric material.

60. A method of making a capacitor, comprising:

forming a layer of forming material;

forming at least one substantially cone-shaped cavity in a surface of the layer of forming material;

forming a first plate of conductive material on the layer of forming material and in the at least one substantially cone-shaped cavity, wherein the first layer of conductive material has a substantially hollow cone-shape conforming to the shape of the cavity;

removing the first plate of conductive material from the surface of the layer of forming material around the cavity;

removing the layer of forming material to a predetermined level to expose at least a portion of an exterior surface of the first plate;

forming a layer of dielectric material on the first plate substantially conforming to the shape of the first plate; and

forming a second plate of conductive material over the layer of dielectric material.

61. A method of making a capacitor, comprising:

forming a layer of forming material;

forming at least one substantially cone-shaped cavity in a surface of the layer of forming material;

forming a isolation wall around the at least one substantially cone-shaped cavity;

forming a photo mask having a predetermined pattern on the isolation wall;

forming a first plate of conductive material on the layer of forming material and in the at least one substantially cone-shaped cavity, wherein the first plate of conductive material has a substantially hollow cone-shape conforming to the shape of the cavity;

removing the first plate of conductive material from the surface of the forming material around the cavity;

removing the photo mask covering the isolation wall;

removing the isolation wall;

removing the layer of forming material to a predetermined level to expose at least a portion of an exterior surface of the first plate;

converting at least one of an interior surface and an exterior surface of the first plate exposed above the layer of forming material to hemispherical grains;

forming a layer of dielectric material on the first plate substantially conforming to the shape of the first plate and the hemispherical grains; and

forming a second plate of conductive material over the layer of dielectric material.

62. A method of making an array of capacitors, comprising:

forming a plurality of first plates of conductive material, each formed in a predetermined shape;

forming a layer of dielectric material on the plurality of first plates and substantially conforming to the shape of each of the first plates; and

a second plate of conductive material formed over the layer of dielectric material.

63. A method of making an array of capacitors, comprising:

forming a layer of forming material;

forming a plurality of cavities in a surface of the layer of forming material, each cavity having a predetermined shape;

forming a plurality of first plates of conductive material on the layer of forming material and in each of the cavities, wherein each first plate is formed in a predetermined shape conforming to the shape of the cavity;

removing the layer of forming material to a predetermined level to expose at least a portion of an exterior surface of each of the first plates above a remaining portion of the layer of forming material;

forming a layer of dielectric material on the first plates substantially conforming to the shape of the first plate; and

forming a second plate of conductive material over the layer of dielectric material.

64. A method of making an array of capacitors, comprising:

forming a first layer of forming material;

forming a nucleation layer on the first layer of forming material;

forming a second layer of forming material on the nucleation layer;

forming a plurality of cavities with a predetermined shape in the first layer of forming material, the nucleation layer and the second layer of forming material;

forming a first plate layer of conductive material on the second layer of forming material and in each of the plurality of cavities, wherein the first plate layer of conductive material forms a predetermined shape conforming to the shape of each of the cavities with a hollow interior surface;

selectively removing portions of the first plate layer of conductive material from the surface of the second layer of forming material from around each of the cavities to form a plurality of first capacitor plates;

removing the second layer of forming material using the first capacitor plates as a mask to expose the nucleation layer and to expose at least a portion of an exterior surface of each first capacitor plate extending above the nucleation layer;

forming a layer of dielectric material on the nucleation layer and on each of the first capacitor plates that substantially conforms to the shape of each of the first capacitor plates; and

forming a second capacitor plate of conductive material over the layer of dielectric material.

65. A method of making an array of capacitors, comprising:

forming a layer of forming material;

forming a plurality of cone-shaped cavities in a surface of the layer of forming material;

forming a isolation wall around the plurality of cavities;

forming a photo mask with a predetermined pattern on the isolation wall;

forming a first plate layer of conductive material on the layer of forming material and in each of the substantially cone-shaped cavities, wherein the first plate layer of conductive material conforms substantially to the shape of each of the cavities;

selectively removing portions the first plate layer of conductive material from the surface of the forming material around each of the cavities to form a plurality of first capacitor plates;

removing the photo mask covering the isolation wall;

removing the isolation wall;

removing the layer of forming material to a predetermined level, using the first capacitor plates as a mask, to expose at least a portion of an exterior surface of each of the first capacitor plates;

converting at least one of an interior surface and an exterior surface of each of the first capacitor plates exposed above the layer of forming material to hemispherical grains;

forming a layer of dielectric material on the layer of forming material and on the first capacitor plates, wherein the dielectric material substantially conforms to the shape of each of the first capacitor plates and the hemispherical grains; and

forming a second capacitor plate of conductive material over the layer of dielectric material.

66. A method of making a memory system, comprising:

forming an array of memory elements; and

forming a capacitor associated with each memory element, wherein forming each capacitor includes:

forming a first plate of conductive material formed in a predetermined shape,

forming a layer of dielectric material formed on at least a portion of the first plate and substantially conforming to the shape of the first plate, and

forming a second plate of conductive material formed over the layer of dielectric material.

67. A method of making a memory system, comprising:

forming an array of memory elements; and

forming a capacitor associated with each memory element, wherein forming each capacitor includes:

forming a first layer of forming material,

forming a nucleation layer on the first layer of forming material,

forming a second layer of forming material on the nucleation layer,

forming at least one cavity with a predetermined shape in the first layer of forming material, the nucleation layer and the second layer of forming material,

forming a first plate of conductive material on the second layer of forming material and in the at least one cavity, wherein the first layer of conductive material forms a predetermined shape conforming to the shape of the cavity with a hollow interior portion,

removing the first plate of conductive material from the surface of the second layer of forming material around the cavity,

removing the second layer of forming material to expose the nucleation layer and to expose at least a portion of an exterior surface of the first plate of conductive material extending above of the nucleation layer,

forming a layer of dielectric material on the first plate that substantially conforms to the shape of the first plate, and

forming a second plate of conductive material over the layer of dielectric material.

68. A method of making a memory system, comprising:

forming an array of memory elements; and

forming a capacitor associated with each memory element, wherein forming each capacitor includes:

forming a layer of forming material,

forming at least one substantially cone-shaped cavity in a surface of the layer of forming material,

forming a first plate of conductive material on the layer of forming material and in the at least one substantially cone-shaped cavity, wherein the first layer of conductive material has a substantially hollow cone-shape conforming to the shape of the cavity,

removing the first plate of conductive material from the surface of the layer of forming material around the cavity,

removing the layer of forming material to a predetermined level to expose at least a portion of an exterior surface of the first plate,

forming a layer of dielectric material on the first plate substantially conforming to the shape of the first plate, and

forming a second plate of conductive material over the layer of dielectric material.

69. A method of making a memory system, comprising:

forming an array of memory elements arranged in rows and columns;

forming a plurality of address lines each coupled to one of a row or a column of memory elements; and

forming a plurality of data lines each coupled to one of a row or a column of memory elements, wherein forming each memory element includes:

forming a transistor including a gate terminal coupled to one of the plurality of address lines and a source/drain terminal coupled to one of the plurality of data lines; and

forming a capacitor coupled to another source/drain terminal of the transistor, wherein forming the capacitor includes:

forming a layer of forming material,

forming a nucleation layer formed on the layer of forming material,

forming a substantially cone-shaped first plate of conductive material including a vertex portion extending through the nucleation layer and partially into the layer of forming material, wherein at least one of an interior surface and an exposed exterior surface of the first plate extending from the layer of forming material and the nucleation layer is converted into hemispherical grains,

forming a layer of dielectric material formed on the nucleation layer and on the interior surface and the exposed exterior surface of the first plate, wherein the layer of dielectric material substantially conforms to the shape of the first plate and the hemispherical grains, and

forming a second plate of conductive material formed over the layer of dielectric material.

70. A method of making a semiconductor die, comprising:

providing a substrate;

forming an integrated circuit supported by the substrate; and

forming a capacitor associated with the integrated circuit, wherein forming the capacitor includes:

forming a first plate of conductive material formed in a predetermined shape,

forming a layer of dielectric material formed on at least a portion of the first plate and substantially conforming to the shape of the first plate, and

forming a second plate of conductive material formed over the layer of dielectric material.

71. A method of making a semiconductor die, comprising:

providing a substrate;

forming an integrated circuit supported by the substrate; and

forming a capacitor associated with the integrated circuit, wherein forming the capacitor includes:

forming a first layer of forming material;

forming a nucleation layer on the first layer of forming material;

forming a second layer of forming material on the nucleation layer;

forming at least one cavity with a predetermined shape in the first layer of forming material, the nucleation layer and the second layer of forming material;

forming a first plate of conductive material on the second layer of forming material and in the at least one cavity, wherein the first layer of conductive

material forms a predetermined shape conforming to the shape of the cavity with a hollow interior surface;

removing the first plate of conductive material from the surface of the second layer of forming material around the cavity;

removing the second layer of forming material to expose the nucleation layer and to expose at least a portion of an exterior surface of the first plate of conductive material extending above of the nucleation layer;

forming a layer of dielectric material on the first plate that substantially conforms to the shape of the first plate; and

forming a second plate of conductive material over the layer of dielectric material.

72. A method of making a semiconductor die, comprising:

providing a substrate;

forming an integrated circuit supported by the substrate; and

forming a capacitor associated with the integrated circuit, wherein forming the capacitor includes:

forming a layer of forming material;

forming at least one substantially cone-shaped cavity in a surface of the layer of forming material;

forming a first plate of conductive material on the layer of forming material and in the at least one substantially cone-shaped cavity, wherein the first layer of conductive material has a substantially hollow cone-shape conforming to the shape of the cavity;

removing the first plate of conductive material from the surface of the layer of forming material around the cavity;

removing the layer of forming material to a predetermined level to expose at least a portion of an exterior surface of the first plate;

converting at least one of an interior surface and an exterior surface of each of the first plates exposed above the layer of forming material to hemispherical grains;

forming a layer of dielectric material on the first plate substantially conforming to the shape of the first plate and the hemispherical grains; and

forming a second plate of conductive material over the layer of dielectric material.

73. A method of making an electronic system, comprising:

forming a processor; and

forming a memory system coupled to the processor and including a plurality of memory cells, wherein forming the memory system includes forming a capacitor associated with each memory cell of the memory system and wherein forming each capacitor includes:

forming a first plate of conductive material formed in a predetermined shape,

forming a layer of dielectric material formed on at least a portion of the first plate and substantially conforming to the shape of the first plate, and

forming a second plate of conductive material formed over the layer of dielectric material.

74. A method of making an electronic system, comprising:

forming a processor; and

forming a memory system coupled to the processor and including a plurality of memory cells, wherein forming the memory system includes forming a capacitor associated with each memory cell of the memory system and wherein forming each capacitor includes:

forming a first layer of forming material;

forming a nucleation layer on the first layer of forming material;

forming a second layer of forming material on the nucleation layer;

forming at least one cavity with a predetermined shape in the first layer of forming material, the nucleation layer and the second layer of forming material;

forming a first plate of conductive material on the second layer of forming material and in the at least one cavity, wherein the first layer of conductive material forms a predetermined shape conforming to the shape of the cavity with a hollow interior surface;

removing the first plate of conductive material from the surface of the second layer of forming material around the cavity;

removing the second layer of forming material to expose the nucleation layer and to expose at least a portion of an exterior surface of the first plate of conductive material extending above of the nucleation layer;

forming a layer of dielectric material on the first plate that substantially conforms to the shape of the first plate; and

forming a second plate of conductive material over the layer of dielectric material.

75. A method of making an electronic system, comprising:

forming a processor; and

forming a memory system coupled to the processor and including a plurality of memory cells, wherein forming the memory system includes forming a capacitor associated with each memory cell of the memory system and wherein forming each capacitor includes:

forming a layer of forming material;

forming at least one substantially cone-shaped cavity in a surface of the layer of forming material;

forming a first plate of conductive material on the layer of forming material and in the at least one substantially cone-shaped cavity, wherein

the first layer of conductive material has a substantially hollow cone-shape conforming to the shape of the cavity;

removing the first plate of conductive material from the surface of the layer of forming material around the cavity;

removing the layer of forming material to a predetermined level to expose at least a portion of an exterior surface of the first plate;

converting at least one of an interior surface and an exterior surface of each of the first capacitor plates exposed above the layer of forming material to hemispherical grains;

forming a layer of dielectric material on the first plate substantially conforming to the shape of the first plate and the hemispherical grains; and

forming a second plate of conductive material over the layer of dielectric material.